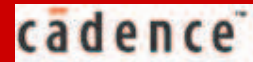


# CeltIC Nanometer Delay Calculator (NDC)



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<b>Title:</b>	CeltIC Nanometer Delay Calculator (NDC) - v6.1	<b>Type:</b>	Instructor Led Course
<b>Product Number:</b>	82131	<b>Price:</b>	\$ 2,100.00 <a href="#">Refund Policy</a>
<b>Length:</b>	2 Day(s)		
<b>Category:</b>	Physical Verification Timing and Extraction Place and Route Design		
<b>Description:</b>	<b>This is an Engineer Explorer course developed for designers familiar with the concepts of signal integrity and delay calculation.</b> In this course, you use CeltIC® NDC to explore and to experiment with the latest delay calculation, crosstalk prevention, crosstalk analysis, as well as repair techniques.		
<b>Learning Objectives:</b>	In this course, you learn to: <ul style="list-style-type: none"><li>• Run noise library characterization to create a .cdB</li><li>• Read and understand noise and delay reports</li><li>• Create an XILM (block) noise model</li><li>• Run CeltIC NDC analysis on a full-chip test case</li><li>• Use the Common Timing Engine (CTE) mode of CeltIC NDC</li></ul>		
<b>Software:</b>	CeltIC® NDC Crosstalk Analyzer with Delay Calculator		
<b>Agenda:</b>	This two-day course covers signal crosstalk and delay theory, as well as the features and use of CeltIC NDC, including these topics: <ul style="list-style-type: none"><li>• Noise impact on functionality and delay</li><li>• Noise library characterization</li><li>• Noise analysis<ul style="list-style-type: none"><li>○ Lab: Characterizing a Noise Library</li><li>○ Lab: Running CeltIC NDC Noise Analysis</li><li>○ Lab: Running CeltIC NDC and Generating Reports</li></ul></li><li>• Noise analysis details</li><li>• Delay analysis<ul style="list-style-type: none"><li>○ Lab: Running a CeltIC NDC Analysis with a Timing Window File</li></ul></li><li>• Hierarchical methodology</li><li>• ECO mode<ul style="list-style-type: none"><li>○ Lab: Creating XILM Models</li><li>○ Lab: Analyzing Hierarchical Noise</li><li>○ Lab: Running CeltIC NDC Analysis in CTE Mode</li></ul></li><li>• Generating SPICE trace and custom reports</li><li>• Virtual attackers and bootstrap noise</li></ul>		
<b>Audience:</b>	ASIC Designers Place and Route Designers Digital IC Designers DSM Designers Chip Designers		
<b>Special Notes:</b>			
<b>Prerequisites:</b>	This course is for designers with practical experience in place and route.		
<b>Related Courses:</b>	<a href="#">SoC Encounter XL RTL-to-GDSII Hierarchical Flow</a> <a href="#">NanoRoute Ultra</a> <a href="#">Library Characterization Using SignalStorm LC</a> <a href="#">VoltageStorm PE Power Analysis</a> <a href="#">VoltageStorm Dynamic Gate (DG)</a>		

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