

Fire & Ice Gate-Level Extraction



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Title:	Fire & Ice QXC Gate-Level Extraction - v5.1.1	Type:	Instructor Led Course
Product Number:	82103	Price:	\$ 700.00 Refund Policy
Length:	1 Day(s)		
Category:	Timing and Extraction Chip Design Back End Physical Design		
Description:	This course introduces you to Fire & Ice® QX gate-level, parasitic extraction technology. You explore the Fire & Ice QX capabilities of parasitic extraction with three-dimensionally accurate extraction to model manufacturing effects, coupled and decoupled capacitance and resistance, and signal integrity effects. You learn to extract accurate gate-level parasitic data to validate the timing of your design and evaluate your signal integrity effects. In addition, you create the technology files and cell libraries for the cell-level extraction.		
Learning Objectives:	<ul style="list-style-type: none">• Learn the overall extraction flow• Review the extraction basics• Perform gate-level extraction• Use the high-accuracy nanometer options• Create cell libraries for the cell-level extraction flow• Create Fire & Ice QX technology files		
Software:	Fire & Ice® QX		
Agenda:	<ul style="list-style-type: none">• Extraction methodology overview• File formats and extraction basics• Gate-level extraction• Creating cell libraries• Creating Fire & Ice QX technology files		
Audience:	Chip Designers Layout Designers Verification Engineers ASIC Designers		
Special Notes:			
Prerequisites:	Familiarity with physical design is recommended.		
Related Courses:	CeltIC Nanometer Delay Calculator (NDC) SoC Encounter XL RTL-to-GDSII Hierarchical Flow		

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