

SoC Encounter XL RTL-to-GDSII Hierarchical Flow



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Title:	SoC Encounter XL RTL-to-GDSII Hierarchical Flow - v5.2	Type:	Instructor Led Course
Product Number:	82114	Length:	2 Day(s)
Category:	Hierarchical Design Synthesis Design Chip Design Place and Route Design		
Description:	In this course, you will explore the SoC Encounter™ XL software, including high-level design planning, virtual prototyping, parasitic extraction, timing optimization, and routing. You will use Tcl commands to prevent, analyze, and fix signal integrity problems. This course uses standard cells and custom blocks to illustrate the Global Physical Synthesis (GPS) features. You will use Tcl scripts and the Encounter® Flow Management System (FMS) to explore the design methodology. This course was formerly called SoC Encounter GPS RTL-to-GDSII Hierarchical Flow.		
Learning Objectives:	In this course, you will <ul style="list-style-type: none">• Run timing optimization• Run silicon virtual prototyping• Run placement• Estimate parasitics and generate delay information• Analyze congestion after running Trial Route• Create clock trees• Create physical partitions (hierarchy) and timing budgets• Run signal integrity analysis• Optimize timing• Run detail routing• Apply postroute timing and signal integrity optimization• Run FMS on a flat design In this course, you will get a high-level technical overview of the SoC Encounter flow. However, to gain in-depth knowledge about each tool, refer to the <i>Related Courses</i> list and take the corresponding course(s).		
Software:	SoC Encounter™ XL		
Agenda:	Day 1 <ul style="list-style-type: none">• Introduction to SoC Encounter XL• Logic synthesis• Silicon virtual prototyping• Hierarchical budget and partitioning Day 2 <ul style="list-style-type: none">• Block implementation• Top implementation• Chip assembly and validation• Flat implementation with FMS		
Audience:	ASIC Designers Digital IC Designers Design Engineers Chip Designers CAD Engineers CAD Developers		
Special Notes:			
Prerequisites:	This course is for designers with practical experience in <ul style="list-style-type: none">• Design methodology• Place and route• First Encounter® XL		
Related Courses:	First Encounter XL NanoRoute Ultra Encounter RTL Compiler CeIIIC Nanometer Delay Calculator (NDC) Encounter Flow Management System VoltageStorm PE Power Analysis		

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